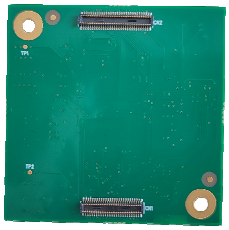
Display Solution
Competence in Digital Visualisation

d.scale-HDIII-MOD

Datasheet

Scaler-Module with
HDMI-/DP-Input & LVDS-Output

3D-Modell (.stp)
available for your
construction



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Date	Rev.	Description	Page
March, 2023	1.0	First draft	
May-08 2023	1.1	Pictures updated,	1, 14
		Signal-description CN1 updated	6
July-03 2023	1.2	3D-view replaced by picture Realtek – RTD2525AR Core Features added	1 4
Oct.-13 2023	1.3	3.2.3 Display & Backlight Control: VL_SW/Selected Voltage corrected	10
Nov.-02 2023	1.4	3.2.1 LVDS Data Channels: Add important note regarding termination of TXBCLK+/- in LVDS single-channel configurations	9

1 General Description

The d.scale-HDIII-MOD is a LCD-TFT controller module based on Realtek's scaler-SOC RTD2525AR. The module measuring only 40 x 40 mm is equipped with 2 board-to-board connectors. While the video signals HDMI/DP together with supply voltage are fed in via one connector, the LVDS and other display control signals are provided at the other connector. To enable the user to flexibly integrate the module into his design, a software tool is available which allows all required configurations and display settings.

2 Features

2.1 Realtek – RTD2525AR Core Features

The d.scale-HDIII-MOD is based on Realtek's multi-function display controller RTD2525A which provides the following core features

- ViviColor™
  - Independent color management (ICM)
  - Dynamic contrast control (DCC)
  - Precise color mapping (PCM)
- Advanced Scaling
  - Advanced zoom algorithm provides high image quality
  - Sharpness/Smooth filter enhancement
  - Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3
- Color Processor
  - True 10 bits color processing engine
  - sRGB compliance
  - Dynamic obvershoot-smear cancelling engine
  - Brightness and contrast control
  - Peaking/Coring function for video sharpness
- DDC/CI, MCCS (Monitor Control Command Set) support
  - Complete OSD-control via DDC/CI
  - Supports several manufacturer (Display Solution GmbH) specific commands
- Embedded OSD
- Audio support, 2ch Audio DAC

2.2 Video Input Interfaces

d.scale-HDIII-MOD supports the following two video-inputs:

- HDMI
  - Operating speed up to 225MHz (up to 60 Hz)
  - HDMI 1.4 support
  - 6-bit, 8-bit, 10-bit and 12-bit color depth transport is supported
  - Optional HDCP1.4 support
- DisplayPort 1.2 via USB Type-C with Alternate Mode support
  - Support 2/4 Lanes up to 1.62Gbps/2.7Gbps/5.4GHz each
  - 6-bit, 8-bit, 10-bit and 12-bit color depth transport
  - Optional HDCP 1.4/HDCP2.2

2.3 LCD-TFT Output Interfaces

d.scale-HDIII-MOD supports LVDS LCD-TFT displays from VGA up to WUXGA and controls the backlight unit.

- LCD-TFT connection
  - Supports LCD-TFTs up to 1920x1200 and pixel clocks up to 93MHz for single LVDS and 186 MHz for dual LVDS
  - Provides single/double pixel LVDS output
  - Support for 8 or 6-bit LVDS (with high-quality dithering)
  - Supports open-LDI and PSWG (VESA) data-mapping on the LVDS-channels
  - User-configurable power-on-sequencing
  - Firmware based +3.3V/+5V GPIO-control for display logic supply
- Backlight control
  - Provides backlight-enable
  - Provides firmware adjustable PWM-signal for brightness-control

2.4 Additional Interfaces and supported peripherals

Since the module is intended to be a turnkey solution for a wide variety of applications, the following interfaces are supported in order to enable peripheral functionalities.

- OSD-control via external Keypad
- Status LEDs
- Audio-output (stereo-headphone)
- I^2C-interface for external sensors like
  - 3-axis Gyro-sensor for Pivot-functionality
  - temperature sensor
  - ambient-light sensor

  to be controlled using DDC/CI (MCCS)

2.5 Control

As usual for a display controller, the d.scale-HDIII-MOD also has an OSD menu. This can be controlled in 2 ways

- 1 + 4 button keypad (power on/off + control)
- VESA-standardized DDC/CI software protocol

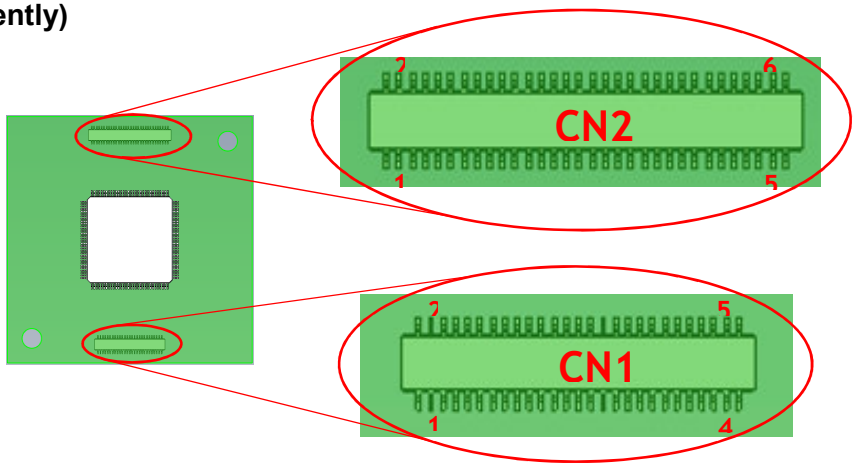
2.6 Power Supply

The d.scale-HDIII-MOD requires a single +5V supply, only. All further required voltages are generated on-board.

3 Details

All the following information refers to the module structure outlined below

The two connectors CN1 & CN2 are shown in the THROUGH-VIEW (the PCB is displayed transparently)



3.1 Input Interfaces - Input-Connector CN1

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	DP_D0+	Lane 0 (positive)
4	DP_AUX-	Auxiliary channel (negative)
5	DP_D0-	Lane 0 (negative)
6	DP_AUX+	Auxiliary channel (positive)
7	GND	Ground
8	GND	Ground
9	DP_D1+	Lane 1 (positive)
10	DP_CAB_DET	DP Cable detect *1
11	DP_D1-	Lane 1 (negative)
12	DP_HPD	Hot plug detect
13	GND	Ground
14	GND	Ground
15	DP_D2+	Lane 2 (positive)
16	SPI_SW_RT	Pull to +3.3V for programming
17	DP_D2-	Lane 2 (negative)
18	SCLK_PRG	Serial clock
19	GND	Ground
20	SDIN_PRG	Serial input
21	DP_D3+	Lane 3 (positive)
22	SDOUT_PRG	Serial output
23	DP_D3-	Lane 3 (negative)
24	SCE_PRG	Chip select
25	GND	Ground

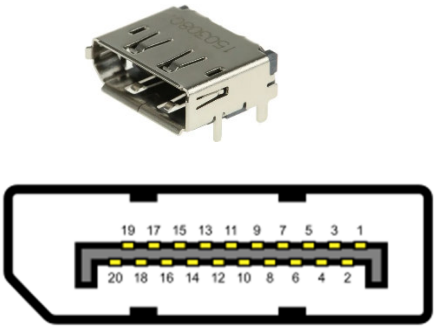
Pin	Signal	Description
26	FLASH_WP	
27	HDMI_RXC-	Differential TMDS Clock-
28	3.3V_PRG	+3.3V supply for programming
29	HDMI_RXC+	Differential TMDS Clock+
30	GND	Ground
31	GND	Ground
32	HDMI_HPD	Hot Plug Detect
33	HDMI_RX0-	Differential TMDS Data 0-
34	HDMI_+5V	+5V/50mA (by graphics card)
35	HDMI_RX0+	Differential TMDS Data 0+
36	HDMI_CAB_DET	HDMI Cable detect *1
37	GND	Ground
38	HDMI_DDC_SDA	DDC EDID data
39	HDMI_RX1-	Differential TMDS data 1-
40	HDMI_DDC_SCL	DDC EDID clock
41	HDMI_RX1+	Differential TMDS data 1+
42	FITP	For internal test purpose *2
43	GND	Ground
44	RFU	Reserved for future use *2
45	HDMI_RX2-	Differential TMDS data 2-
46	+5.0V	Module power supply
47	HDMI_RX2+	Differential TMDS data 2+
48	+5.0V	Module power supply
49	GND	Ground
50	+5.0V	Module power supply

*1 Can be connected to one of the cable GND-pins to detect cable-connection. If not used please connect to GND

*2 Do not connect.

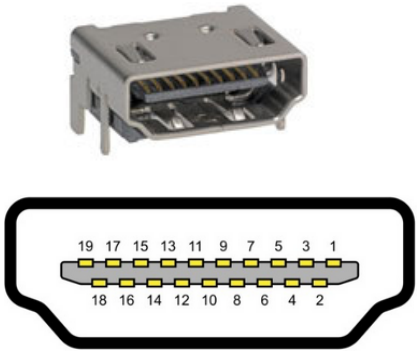
3.1.1 Reference Pin-Assignments

DisplayPort



Pin	Signal	Description
1	DP_D0+	Lane 0 (positive)
2	GND	Lane 0 Shield - Ground
3	DP_D0-	Lane 0 (negative)
4	DP_D1+	Lane 1 (positive)
5	GND	Lane 1 Shield - Ground
6	DP_D1-	Lane 1 (negative)
7	DP_D2+	Lane 2 (positive)
8	GND	Lane 2 Shield - Ground
9	DP_D2-	Lane 2 (negative)
10	DP_D3+	Lane 3 (positive)
11	GND	Lane 3 Shield - Ground
12	DP_D3-	Lane 3 (negative)
13	Config1	Connected to GND
14	Config2	Connected to GND
15	DP_AUX+	Auxiliary Channel (positive)
16	GND	Aux Shield - Ground
17	DP_AUX-	Auxiliary Channel (negative)
18	DP_HPD	Hot Plug Detect
19	Return (GND)	Return for Power
20	DP_PWR	Power for Connector (3.3V/500mA)

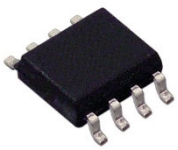
HDMI



Pin	Signal	Description
1	TMDS2+	Differential TMDS Data 2+
2	GND	TMDS Data2 Shield - Ground
3	TMDS2-	Differential TMDS Data 2-
4	TMDS1+	Differential TMDS Data 1+
5	GND	TMDS Data1 Shield
6	TMDS1-	Differential TMDS Data 1-
7	TMDS0+	Differential TMDS Data 0+
8	GND	TMDS Data0 Shield
9	TMDS0-	Differential TMDS Data 0-
10	TMDSCLK-	Differential TMDS Clock-
11	GND	TMDS Clock Shield
12	TMDSCLK+	Differential TMDS Clock+
13	RSV	Reserved
14	RSV	Reserved
15	SCL	DDC EDID clock
16	SDA	DDC EDID data
17	DDC/CEC GND	Ground
18	+5V	+5V/50mA (by graphics card)
19	HPD	HotPlug Detect

Programming Interface

The firmware of the scaler SOC (RTD2525AR) including required EDID-files (DP/HDMI) can be programmed via the CN1 connector using e.g. a standard Chip-Programmer.



IC Pin	Signal	Description
1	CS#	Chip select
2	SO	Serial output
3	WP#	Write protect (is pulled high)
4	GND	Ground
5	SI	Serial input
6	SCK	Serial clock
7	Hold#	Hold (is pulled high)
8	VDD	Device power supply

SPI_PRG
This pin has to be pull to +3.3V to connect the SPI-Flash device of the d.scale-HDIII-MOD to the programming interface of CN1

SPI_V_PRG
If an external CHIP-programmer is used, usually the SPI-Flash chip supply can be connected to this pin. This pin does not have to be powered, if the d.scale-HDIII-module is powered up via CN1 pins 46, 48, 50.

3.1.2 Power Supply

On pins 48, 49 and 50 a 5.0V supply voltage has to be provided to power up the d.scale-HDIII-MOD. Please see the "Electrical Characteristics" for power consumption and tolerances.

3.2 Output Interfaces - Output-Connector CN2

Pin	Signal	Description
1	FITP	For internal test purpose *1
2	GND	Ground
3	KEY_REF	Keypad reference voltage *2
4	TXA0-	LVDS / Channel-1 / Data-Pair-0
5	RFU	Reserved for future use *1
6	TXA0+	LVDS / Channel-1 / Data-Pair-0
7	RFU	Reserved for future use *1
8	GND	Ground
9	RFU	Reserved for future use *1
10	TXA1-	LVDS / Channel-1 / Data-Pair-0
11	GND	Ground
12	TXA1+	LVDS / Channel-1 / Data-Pair-0
13	KEY	OSD Keypad Input
14	GND	Ground
15	LED1	Status-LED 1
16	TXA2-	LVDS / Channel-1 / Data-Pair-0
17	LED2	Status-LED 2
18	TXA2+	LVDS / Channel-1 / Data-Pair-0
19	RFU	Reserved for future use *1
20	GND	Ground
21	RFU	Reserved for future use *1
22	TXACLK-	LVDS / Channel-1 / Clock-Pair
23	GND	Ground
24	TXACLK+	LVDS / Channel-1 / Clock-Pair
25	ENVCC	Enable display logic supply
26	GND	Ground
27	VL_SW	Display logic supply select
28	TXA3-	LVDS / Channel-1 / Data-Pair-3
29	BRC_PWM	Brightness-control PWM-signal
30	TXA3+	LVDS / Channel-1 / Data-Pair-3

Pin	Signal	Description
31	ENBKL	Enable display backlight
32	GND	Ground
33	GND	Ground
34	TXB0-	LVDS / Channel-2 / Data-Pair-0
35	RFU	Reserved for future use *1
36	TXB0+	LVDS / Channel-2 / Data-Pair-0
37	PERI_SCL	I^2C-clock for Peripherals
38	GND	Ground
39	PERI_SDA	I^2C-data for Peripherals
40	TXB1-	LVDS / Channel-2 / Data-Pair-1
41	GND	Ground
42	TXB1+	LVDS / Channel-2 / Data-Pair-1
43	RFU	Reserved for future use *1
44	GND	Ground
45	RFU	Reserved for future use *1
46	TXB2-	LVDS / Channel-2 / Data-Pair-2
47	RFU	Reserved for future use *1
48	TXB2+	LVDS / Channel-2 / Data-Pair-2
49	RFU	Reserved for future use *1
50	GND	Ground
51	GND	Ground
52	TXBCLK-	LVDS / Channel-2 / Clock-Pair
53	AUDIO_HOUT L	Headphone-output, left
54	TXBCLK+	LVDS / Channel-2 / Clock-Pair
55	AUDIO_HOUT R	Headphone-output, right
56	GND	Ground
57	RFU	Reserved for future use *1
58	TXB3-	LVDS / Channel-2 / Data-Pair-3
59	GND	Ground
60	TXB3+	LVDS / Channel-2 / Data-Pair-3

*1 Do not connect

*2 This pin is a +3.3V output which can be used as keypad reference voltage. Maximum output is 25mA

3.2.1 LVDS-Data Channels

The d.scale-HDIII-MOD provides one or two LVDS data channels and supports 6-bit and 8-bit (per colour) displays.

Single channel
Usually LCD-TFT displays with resolutions from VGA (640x480) up to XGA (1024x768) / WXGA (1366x768) are equipped with a single channel LVDS interface whereas with each clock-cycle the data for one pixel is transmitted

These displays have to be connected to the **TXA...- Channel**

> **NOTE:**
> If a LCD-TFT display with single-channel LVDS is connected it is essential to ensure that the TXBCLK+/- differential pair is terminated with a 100 Ohm resistor.
> - If only single channel LVDS is used in the design, please place the terminating resistor close to CN2
> - If single and dual channel LVDS is used in the design, please place the terminating resistor close to the design's output connector.

Dual channel
LCD-TFT displays with resolutions from SXGA (1280x1024) up to FHD (1280x1080) / WUXGA (1920x1200) are equipped with a dual channel LVDS interface, whereas with each clock-cycle the data for two pixels is transmitted

These displays have to be connected to the **TXA...- Channel** **&** **TXB…- Channel**

NOTE
TXA...- Channel
This channel provides the data for the 1. / 3. / 5. / … pixel

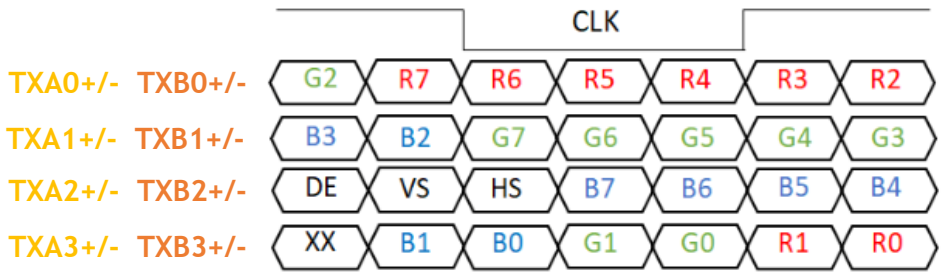
TXB…- Channel
This channel provides the data for the 2. / 4. / 6. / … pixel

3.2.2 LVDS Data Mapping

Historically, 2 LVDS data mappings have been established, known by different names

***Data-Mapping-1* known as:**
- Conventional data-mapping
- Open-LDI data-mapping
- JEIDA data-mapping

Characteristics
The LVDS data-pairs TXA3+/- & TXB3+/- transmits the LSBits of each color namely Red-0/Red-1, Green-0/Green-1, Blue-0/Blue-1



Color-Depth

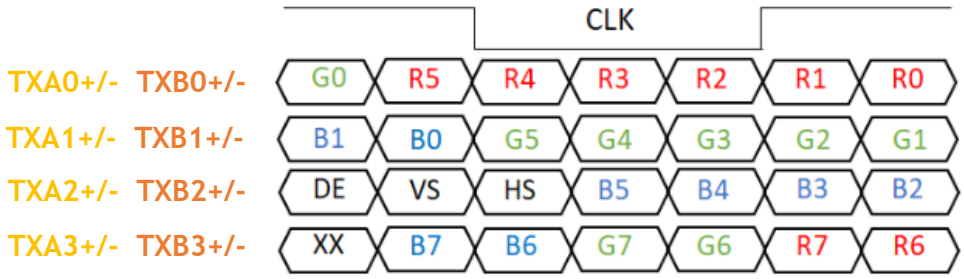
- Displays with 18-bit color-depth (262K colors) requires TX..0+/- to TX..2+/-
- Displays with 24-bit color-depth (16Mio colors) requires TX..0+/- to TX..3+/-

***Data-Mapping-2* known as:**

- Non-Conventional data-mapping
- VESA data-mapping

Characteristics

The LVDS data-pairs TXA3+/- & TXB3+/- transmits the MSBits of each color namely Red-6/Red-7, Green-6/Green-7, Blue-6/Blue-7



Color-Depth

This data-mappings supports 24-bit color depth (16Mio colors), ONLY.

3.2.3 Display & Backlight Control

In order control the LCD-TFT display and the according backlight the following signals are provided. The power-on/off sequence is controlled by firmware and can be adjusted by the user.

ENVCC

ENVCC is used to enable the supply voltage of the display logic and features the following characteristics:

- Active high
- Push/pull
- +3.3V signal level

VL_SW

VL_SW can be used to ensure by an user configurable firmware setting, that the correct logic-supply voltage is provided to the connected display. Usually it is used to adjust the voltage either to +3.3V or +5.0V.

VL_SW	Selected Voltage
High	+5.0V
Low	+3.3V

VL_SW has the following characteristics:

- Push/pull
- +3.3V signal level

ENBKL

ENBKL is used to enable the backlight inverter circuitry and has the following characteristics:

- Active high
- Push/pull
- +3.3V signal level

BRC_PWM

BRC_PWM is a pulse-width-modulated signal which is used to control the panel's backlight brightness. The PWM-characteristics (e.g. frequency, min/max, etc.) can be adjusted by the user via firmware settings. The signal features the following characteristics:

- Positive PWM
- Push/pull
- +3.3V signal level

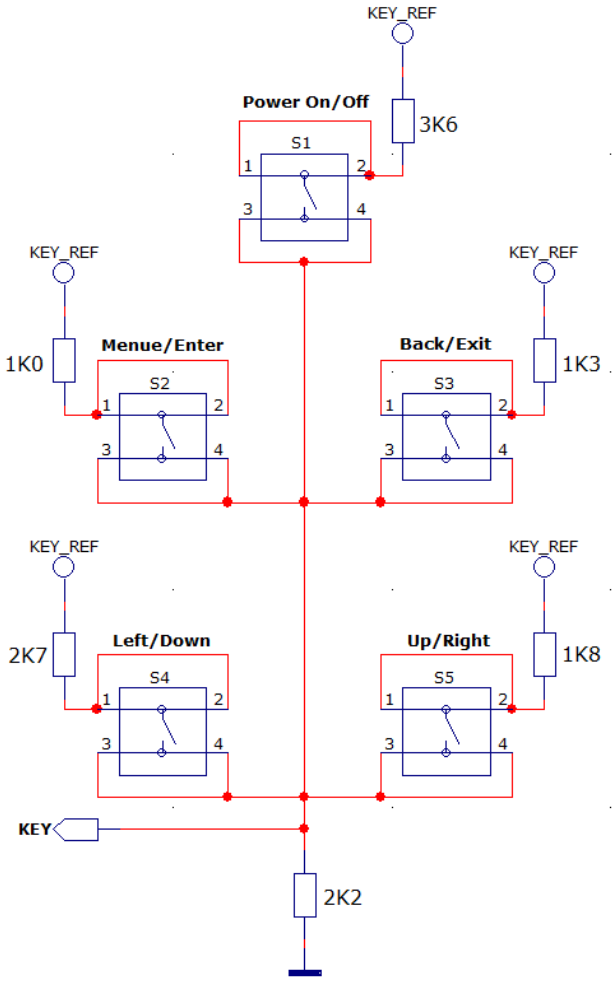
3.2.4 Scaler Control & Status

Keypad

The d.scale-HDIII-MOD supports an external keypad to control the OSD-menu. It supports the following buttons:

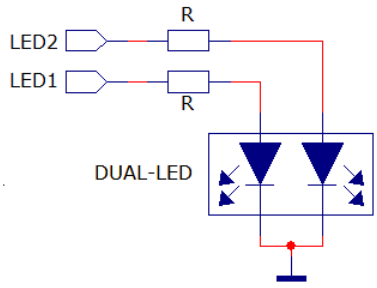
- Button S1 for power on/off the scaler,
- Button S2 to enter the menu respectively confirm selection
- Button S3 to exit the menu respectively to go one step back
- Button S4 to move left/down respectively decrease the selected value depending on the selected menu status
- Button S5 to move right/up respectively increase the selected value depending on the selected menu status

Depending on the key pressed, the voltage value returned via KEY is evaluated. Below the required resistor values are shown. The reference voltage KEY_REF is +3.3V and can be drawn from the KEY_REF pin.



Status LEDs

In order to show different system states two GPIOs (push-pull, max.10mA) are available. These GPIOs are provided on CN2 on pins LED1 and LED2. The table below shows the states.



Description	LED1	LED2
Power-off / Standby	Off	Off
Power-on / System start-up, splash-screen is displayed Power-on / No valid video input detected	Off	On
Power-on / Valid video input detected	On	Off
Power-on / no valid video input detected / go to sleep	On	On

3.2.5 Peripherals

I²C-Interface

The d.scale-HDIII-MOD provides an I²C-Interface for connection of useful peripheral devices. The devices can be controlled via the DDC/CI (MCCS) which is a standardized channel by VESA. As physical interface the DDC (HDMI) or the AUX-channel (DisplayPort) is used, which means, that no additional connection like USB or UART is required. The user can select and configure the devices in the firmware configuration tool.

Currently the following devices are supported:

- STMIcro / LIS3DH
  3-axis Gyro-sensor for Pivot-functionality
- Texas Instruments / TMP102
  Temperature sensor
- Texas Instruments / OPT3001
  ambient-light sensor

Analog Audio output

Via the two pins AUDIO_HOUTL and AUDIO_HOUTR an analog stereo headphone signal is provided.

4 Connector Overview

CN	Description	Type	Manufacturer
CN1	Input	DF40C-50DP-04V(51)	Hirose
CN2	Output	DF40C-60DP-04V(51)	Hirose

5 Specifications

5.1 Electrical Characteristics

Operating Values

Table below shows typical operating values:

Item	Condition	MIN.	TYP.	MAX.	Unit	Note
Supply Voltage		4.75	5.0	5.25	VDC	
Current Input			200		mA	

5.2 Temperature & Humidity

Item	MIN.	TYP.	MAX.	Unit	Note
Operating Temperature	0/TBD	-	+70	°C	
Storage Temperature	10/TBD	-	+85	°C	
Humidity	5	-	90	%RHmax	

6 Outline Dimensions