FE12.1

USB 2.0 HSIC HIGH SPEED 7-PORT HUB CONTROLLER

Product Brief

INTRODUCTION

The Terminus FE12.1 HSIC (*High-Speed Inter-Chip*) High Speed 7-Port Hub is an USB 2.0 hub controller with HSIC upstream connectivity and seven downstream ports, including five USB 2.0 ports and two HSIC ports.

HSIC has been designed to replace a standard USB PHY and USB Cable with an interface that is optimized for circuit board layout. An USB chip-to-chip interconnection makes use of 2-signal (Strobe, Data) source-synchronous serial interface to achieve. Upstream of the FE12.1 is HSIC interface, and it is intended to be used for embedded USB applications where low-power, high performance, and low costs are design requiremets.

The FE12.1 is a highly integrated, high quality, high performance, low power consumption, yet low cost solution for USB 2.0 HSIC High Speed 7-Port Hub.

It adopts Multiple Transaction Translator (MTT) architecture to explore the maximum possible throughput. Six, instead of two, non-periodic transaction buffers are used to minimize potential traffic jamming. The whole design is based on state-machine-control to reduce the response delay time; no micro controller is used in this chip.

To guarantee high quality, the whole chip is covered by *Test Scan Chain* – even on the high speed (480MHz) modules, so that all the logic components could be fully tested before shipping. Special Build-In-Self-Test mode is designed to exercise HSIC ports and all high, full, and low speed Analog Front End (AFE) components on the packaging and testing stages as well.

Low power consumption is achieved by using LPM (*Link Power Management*) feature and comprehensive power/clock control mechanism. Most part of the chip will not be clocked unless needed.

The FE12.1 could be optionally configured to support Charging Downstream Ports (which are only enabled on standard USB ports) as defined by USB-IF *Battery Charging Specification*. With this feature enabled, an USB hub could be easily transformed into a charging station – *USB Charging Hub* for *Universal Charging Solution* compliant battery based portable devices.

A practical example is shown in Figure 1. FE12.1 expands the USB devices through the HSIC interface of the SOC. For one thing, the idle HSIC ports of SOC can be fully utilized; for another, the SOC's native USB ports can be exclusively used to connect to external devices, such as mobile phones, tablets, and so on.

FEATURES

- Fully compliant with High-Speed Inter-Chip USB Electrical Specification Version 1.0 (HSIC);
  - □ Upstream facing port supports High-Speed (480MHz);
  - □ 2 downstream facing ports (Port 5,6) support High-Speed (480MHz);

- Fully compliant with Universal Serial Bus Specification Revision 2.0 (USB 2.0);
  - □ 5 downstream facing ports (Port 1,2,3,4,7) support High-Speed (480MHz), Full-Speed (12MHz), and Low-Speed (1.5MHz) modes;

- Compliant with Universal Charging Solution, and USB Battery Charging Specification 1.1/1.2;

- USB Link Power Management (LPM) support;

- Integrated HSIC Transceivers;

- Integrated USB 2.0 Transceivers;

- Integrated downstream 15KΩ pull-down, and serial resisters;

- Integrated 3.3V to 1.8V regulator;

- Integrated Power-On-Reset circuit;

- Integrated 12MHz Oscillator with feedback resister, and crystal load capacitance;

- Integrated 12MHz-to-480MHz Phase Lock Loop (PLL);

- Integrated Portable Device detection circuitry for UCS supporting;

- *Multiple Transaction Translators* (MTT) –
  - □ One TT for each downstream port;
  - □ Alternate Interface 0 for Single-TT, and Alternate Interface 1 for Multiple-TT;
  - □ Each TT could handle 64 periodic Start-Split transactions, 32 periodic Complete-Split transactions, and 6 none-periodic transactions;

- Support Self-Powered Mode only;

- Board configure support of portable device detection mechanism for Universal Charging Solution on 5 downstream ports (USB 2.0);